IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An integrated circuit comprising:

a clock input pad to receive an input clock signal;

a clock output pad to transmit an output clock signal; ~~and~~

a loop circuit to phase lock the input clock signal and the output clock signal[[.]];

a slave circuit responsive to the loop circuit to produce a first clock signal having a phase substantially equal to the output clock signal and a second clock signal having a phase offset substantially 90 degrees from the first clock signal; and

an output multiplexer having control inputs coupled to be responsive to the first and second clock signals, and having data inputs coupled to receive four separate phases of data signals.

2. (Original) The integrated circuit of claim 1 wherein the loop circuit includes a phase detector to compare phases of the input clock signal and the output clock signal.

3. (Original) The integrated circuit of claim 2 further comprising a clock generator to generate a plurality of clock signals of different phases from the input clock signal.

4. (Original) The integrated circuit of claim 3 wherein the loop circuit further comprises a first phase interpolator to generate the output clock signal from the plurality of clock signals from the clock generator.

5. (Original) The integrated circuit of claim 4 wherein the loop circuit further comprises control logic to influence operation of the first phase interpolator in response to the phase detector.

6. (Currently Amended) The integrated circuit of claim 5, wherein the slave circuit further ~~comprising~~ comprises a delay line responsive to the clock generator.

7. (Currently Amended) The integrated circuit of claim 6, wherein the slave circuit further ~~comprising~~ comprises at least one other phase interpolator coupled to the delay line to generate the first and second clock signals. ~~at least one clock signal to time output data off the integrated circuit.~~

8. (Currently Amended) The integrated circuit of claim 7 wherein the operation of the at least one other phase interpolator is influenced by the ~~PI~~ control logic.

9. (Canceled)

10. (Currently Amended) The integrated circuit of claim [[9]] 1 wherein the loop circuit includes a dummy output multiplexer having a delay characteristic substantially equivalent to the output multiplexer.

11. (Currently Amended) An integrated circuit comprising:

a clock input pad to receive an input clock;

a clock output pad to transmit an output clock;

a data output pad to transmit a data signal;

a loop circuit to phase align the output clock with the input clock where the output clock is derived from the input clock; and

data output circuitry including an output multiplexer coupled to drive the data output pad, the multiplexer having a control input coupled to receive a clock signal related to ~~to time data off the integrated circuit using~~ the output clock.

12. (Original) The integrated circuit of claim 11 wherein the loop circuit includes a phase-locked loop to generate the output clock.

13. (Original) The integrated circuit of claim 12 further comprising clock routing circuitry having a first delay characteristic coupled between the clock input pad and the phase-locked loop.

14. (Original) The integrated circuit of claim 13 further comprising clock routing circuitry having a second delay characteristic coupled between the phase-locked loop and the clock output pad.

15. (Original) The integrated circuit of claim 14 wherein the phase-locked loop comprises a feedback path having both the first and second delay characteristics.

16. (Currently Amended) A method comprising:

receiving an input clock signal;

providing the input clock signal to a clock generator;

interpolating between phases of clock signals provided by the clock generator to produce an output clock signal; ~~and~~

phase locking the input clock signal to the output clock signal by modifying the interpolating[[.]]; and

interpolating between phases to produce at least one clock signal to time data off the integrated circuit, wherein the at least one clock signal comprises two clock signals to time data off the integrated circuit at four times the rate of the output clock signal.

17-18. (Canceled).

19. (Currently Amended) The method of claim ~~18~~ 16 further comprising multiplexing between four data signals using the two clock signals.

20. (Currently Amended) An electronic system comprising:

an antenna;

a radio frequency circuit coupled to the antenna;

a memory device; and

a controller coupled to the radio frequency circuit and the memory device, the controller including a clock input pad to receive an input clock signal, a clock output pad to transmit an

output clock signal, ~~and~~ a loop circuit to phase lock the input clock signal and the output clock signal[[.]], a slave circuit responsive to the loop circuit to produce a first clock signal having a phase substantially equal to the output clock signal and a second clock signal having a phase offset substantially 90 degrees from the first clock signal, and an output multiplexer having control inputs coupled to be responsive to the first and second clock signals, and having data inputs coupled to receive four separate phases of data signals.

21. (Original) The electronic system of claim 20 wherein the loop circuit includes a phase detector to compare phases of the input clock signal and the output clock signal.

22. (Original) The electronic system of claim 21 wherein the controller further comprises a clock generator to generate a plurality of clock signals of different phases from the input clock signal.

23. (Original) The electronic system of claim 22 wherein the loop circuit further comprises a first phase interpolator to generate the output clock signal from the plurality of clock signals from the clock generator.